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Application No. 10/708,066	Filing Date 02/06/2004	Examiner B. CHERVINSKY	Group Art Unit 2835

Invention: METHOD AND STRUCTURE FOR HEAT SINK ATTACHMENT IN SEMICONDUCTOR DEVICE PACKAGING

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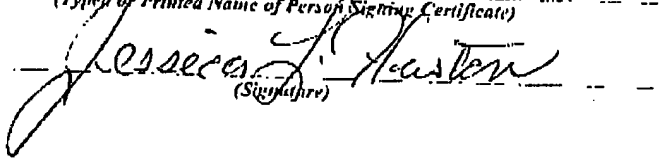
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TRANSMITTAL OF APPEAL BRIEF (Large Entity)	Docket No. FIS920030398US1

In Re Application Of: ROGER LAM ET AL.

Application No.	Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.
10/708,066	02/06/2004	B. CHERVINSKY	29371	2835	2065

Invention: METHOD AND STRUCTURE FOR HEAT SINK ATTACHMENT IN SEMICONDUCTOR DEVICE PACKAGING

COMMISSIONER FOR PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on November 3, 2005

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Dated: December 22, 2005

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	ROGER LAM, ET AL.	) Group Art Unit: 2835
Serial No.:	10/708,066	)
Filed:	February 6, 2004	) Examiner: Chervinsky, B.
For:	METHOD AND STRUCTURE FOR HEAT SINK ATTACHMENT IN SEMICONDUCTOR DEVICE PACKAGING	) Confirmation No.: 2065

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APPEAL BRIEF

1. REAL PARTY IN INTEREST

The real party in interest in this Appeal is the assignee, International Business Machines Corporation.

2. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known at this time to the Appellants, or to the Appellants' legal representatives that will directly affect, or be directly affected by, or have a bearing upon the Board's decision in this appeal.

3. STATUS OF THE CLAIMS

Claims 1-20 stand rejected as more fully set forth below. The final rejection of claims 1-20 is appealed.

4. STATUS OF AMENDMENTS

No amendments have been filed subsequent to the Final Office Action of August 3, 2005. A copy of the appealed claims is provided in a Claims Appendix attached hereto.

5. SUMMARY OF THE CLAIMED SUBJECT MATTER

Pursuant to MPEP §1205, a concise explanation of the subject matter defined in each of the independent claims involved in the appeal is provided with reference to the specification and drawings. It is understood that the reference to the specific embodiments in the specification and drawings is provided for compliance with MPEP §1205 and is not intended to limit the scope of the claims.

Claim 1 is directed toward a heat sink attachment structure as shown in Figure 2. The structure features an integrated circuit chip (106) mounted on a substrate surface (e.g., module 102 in Figure 2), and a thermal interface layer (110) in contact with the integrated circuit chip (106). (***specification, paragraphs [0017]-[0018]***). A heat sink (112) is in contact with the thermal interface layer (110), and at least one spacer member (202) is in contact between the substrate surface (102) and the heat sink (112). The spacer member (202) is provided with an adhesive material (204) on top and bottom surfaces thereof. (***specification, paragraph [0020]***).

Claim 8 is directed toward a method for implementing attachment of a heat sink to an integrated circuit chip as shown in Figure 4. The method includes applying a thermal interface layer to the chip (402), and adhesively applying a first side of at least one spacer member to a substrate to which the chip is mounted (404). The heat sink is

aligned to the chip (406), and a load is applied to the heat sink until the heat sink is adhesively bonded to a second side of the at least one spacer member (408). (*specification, paragraph [0025]*).

Claim 14 is directed toward a heat sink attachment structure as shown in Figure 2. The structure features a chip module (102) mounted on a circuit board substrate (104). At least one integrated circuit chip (106) mounted on the chip module (102), and a thermal interface layer (110) is in contact with the integrated circuit chip (106). (*specification, paragraphs [0017]-[0018]*). A heat sink (112) is in contact with the thermal interface layer (110), and at least one spacer member (202) is in contact between the substrate surface (102) and the heat sink (112). The spacer member (202) is provided with an adhesive material (204) on top and bottom surfaces thereof. (*specification, paragraph [0020]*).

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The grounds of rejection to be reviewed on appeal are:

(A) whether the Examiner's rejection of claims 1, 4, 6, 8, 11, 14, 17 and 19 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent 6,218,730 to Toy, et al. is improper; and

(B) whether the Examiner's rejection of claims 3, 5, 7, 10, 12, 13, 16, 18 and 20 under 35 U.S.C. §103(a) as being unpatentable over Toy, et al., and whether the Examiner's rejection of claims 2, 9 and 15 under 35 U.S.C. §103(a) as being unpatentable over Toy, et al., in view of U.S. Patent 6,730,993 to Boyer, et al. is improper.

7. ARGUMENT

A. Claims 1, 4, 6, 8, 11, 14, 17 and 19 are patentable under 35 U.S.C. §102(b) over U.S. Patent 6,218,730 to Toy, et al.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

In the present application, the Examiner has failed to establish a *prima facie* case in support of the §102(b) rejections for the reason that Toy does not teach or suggest "at least one spacer member in contact between said substrate surface and said heat sink..." as claimed in the instant application.

In support of the present rejections, the Examiner states that Toy discloses "...a heat sink 20 in contact with the thermal interface layer 17 and at least one spacer member 47 in contact between said chip module 10 and the heat sink...". However, a review of the Toy reference indicates that element 20 is not described as a heat sink, but is in fact primarily a lid for environmental protection of the substrate mounted chip. Moreover, a separate, distinct heat sink component is specifically shown and discussed in Toy, as designated by the reference numeral 50 in Figure 1. In fact the heat sink 50 is shown attached to the lid 20 through a conductive adhesive 51, which provides a distinction between the two components (See, for example, column 5, lines 37-44).

In the Final Office Action, the Examiner states in response (on paragraph 6, pages 3-4) "the elements 20, 51 and 50 in combination can be considered as the heat sink because their primary function is to dissipate heat generated by the IC chip 16." (Emphasis added) However, it is respectfully submitted by the Applicants that there is no support for such an interpretation in the Toy reference and, as such, the basis for the Examiner's rejections is erroneous.

This is not an instance where the Toy reference teaches a claimed element, but simply uses a different term to describe that element. Rather, Toy explicitly discloses, in one embodiment, a "heat sink" which is clearly depicted as element 50 in Figure 1 of the

Toy reference. Moreover, it is seen that the Toy heat sink 50 is not actually in contact with the "spacer member" 47 identified by the Examiner. Instead, the Examiner has erroneously attempted to expand the definition of "heat sink" to cover the combination of the lid 20, the conductive adhesive 51, and the heat sink 50 .

Nowhere in the Toy reference is it indicated that the heat sink comprises elements 20, 50 and 51 together. Nor does Toy indicate the primary function of the lid 20 is to dissipate heat generated by the IC chip 16. In fact, the lid 20 is described as being "for environmental and handling protection." (Col. 5, lines 39-40) Although lid 20 and adhesive 51 can act as a thermally conductive medium through which heat generated by the chip can be ultimately carried to the heat sink 50, neither the lid 20 nor the adhesive 51 acts as the ***heat sink*** itself. Although it is acknowledged in the Figure 5 embodiment of Toy that lid 20 can operate as a "thermal spreader," this is still not the equivalent of a "heat sink" as one skilled in the art will recognize a distinction between the two. Whereas a thermal spreader may more evenly distribute heat from a source, it is the heat sink (e.g., through fins) that ultimately dissipates the distributed heat (e.g., from a thermal spreader) to the ambient. Thus, a distinction in functionality between the two exists.

Accordingly, since the claims of the instant application recite that the spacer member is in contact between the substrate surface and the heat sink, a determination that Toy meets this element is in clear error because the lid 20 is not a heat sink. The Applicants therefore respectfully submit that because the Toy reference fails to teach or suggest at least one spacer member in contact between a substrate surface and a heat sink, the §102(b) rejections of claims 1, 4, 6, 8, 11, 14, 17 and 19 should be reversed.

B. Claims 3, 5, 7, 10, 12, 13, 16, 18 and 20 are patentable under 35 U.S.C. §103(a) over Toy, et al., and claims 2, 9 and 15 are patentable under 35 U.S.C. §103(a) over Toy, et al., in view of U.S. Patent 6,730,993 to Boyer, et al.

For an obviousness rejection to be proper, the Examiner must meet the burden of

establishing that (1) all elements of the claimed invention are disclosed in the prior art; (2) that the prior art relied upon, coupled with knowledge generally available in the art at the time of the invention, must contain some suggestion or incentive that would have motivated the skilled artisan to modify a reference or to combine references; and (3) that the proposed modification of the prior art must have had a reasonable expectation of success, determined from the vantage point of the skilled artisan at the time the invention was made. *In re Fine*, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988); *In Re Wilson*, 165 U.S.P.Q. 494, 496 (C.C.P.A. 1970); *Amgen v. Chugai Pharmaceuticals Co.*, 927 U.S.P.Q.2d, 1016, 1023 (Fed. Cir. 1996).

Thus, under the first element, to establish *prima facie* obviousness of a claimed invention, all of the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). "All words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970). Because a prima facie case for the §102(b) rejection of independent claims 1, 8 and 14 has not been established, for the reasons set forth above, any §103 rejections based on Toy are also erroneous.

As such, the §103 rejections of claims 2, 3, 5, 7, 9, 10, 12, 13, 15, 16, 18 and 20 should therefore also be reversed.

9. CONCLUSION

For the above stated reasons, it is respectfully requested that the rejections of claims 1-20, under each of the grounds outlined in the Final Office Action of August 3, 2005, be reversed. If any fees are due with respect to this Appeal, please charge them to Deposit Account No. 09-0458 maintained by Applicants' attorneys.

Respectfully submitted,
ROGER LAM, ET AL.

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Appendix -CLAIMS

1. A heat sink attachment structure, comprising:

an integrated circuit chip mounted on a substrate surface;

a thermal interface layer in contact with said integrated circuit chip;

a heat sink in contact with said thermal interface layer; and

at least one spacer member in contact between said substrate surface and said heat sink, wherein said at least one spacer member is provided with an adhesive material on top and bottom surfaces thereof.

2. The structure of claim 1, wherein said at least one spacer member comprises a rigid material of a generally cylindrical shape.

3. The structure of claim 2, wherein said at least one spacer member comprises phenolic.

4. The structure of claim 1, wherein said thermal interface layer is adhesive free.

5. The structure of claim 1, wherein said adhesive material provided on said at least one spacer member comprises a reworkable epoxy curable at room temperature.

6. The structure of claim 1, wherein said thermal interface layer further comprises a thermal interface pad.

7. The structure of claim 6, wherein said thermal interface pad has an initial thickness of about 6 mil and a compressed thickness of about 4 mils.

8. A method for implementing attachment of a heat sink to and integrated circuit chip, the method comprising:

applying a thermal interface layer to the chip;

adhesively applying a first side of at least one spacer member to a substrate to which the chip is mounted;

aligning the heat sink to the chip; and

applying a load to the heat sink until the heat sink is adhesively bonded to a second side of said at least one spacer member.

9. The method of claim 8, wherein said at least one spacer member comprises a rigid material of a generally cylindrical shape.

10. The method of claim 9, wherein said at least one spacer member comprises phenolic.

11. The method of claim 8, wherein said thermal interface layer is adhesive free.

12. The method of claim 8, wherein said adhesive material provided on said at least one spacer member comprises a reworkable epoxy curable at room temperature.

13. The method of claim 8, wherein said thermal interface layer further comprises a thermal interface pad having an initial thickness of about 6 mil and a compressed thickness of about 4 mils.

14. A semiconductor device packaging assembly, comprising:

a chip module mounted on a circuit board substrate;

at least one integrated circuit chip mounted on said chip module;

a thermal interface layer in contact with said at least one integrated circuit

chip;

a heat sink in contact with said thermal interface layer; and

at least one spacer member in contact between said chip module and said heat sink, wherein said at least one spacer member is provided with an adhesive material on top and bottom surfaces thereof.

15. The semiconductor device packaging assembly of claim 14, wherein said at least one spacer member comprises a rigid material of a generally cylindrical shape.

16. The semiconductor device packaging assembly of claim 15, wherein said at least one spacer member comprises phenolic.

17. The semiconductor device packaging assembly of claim 14, wherein said thermal interface layer is adhesive free.

18. The semiconductor device packaging assembly of claim 14, wherein said adhesive material provided on said at least one spacer member comprises a reworkable epoxy curable at room temperature.

19. The semiconductor device packaging assembly of claim 14, wherein said thermal interface layer further comprises a thermal interface pad.

20. The semiconductor device packaging assembly of claim 19, wherein said thermal interface pad has an initial thickness of about 6 mil and a compressed thickness of about 4 mils.